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EXAMINER	
CHOW, CHARLES CHIANG	
ART UNIT	**PAPER NUMBER**
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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/617,469	KRISHNAMURTHI, KATHIRAVAN	
	Examiner	Art Unit	
	Charles Chow	2685	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *10 July 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-24* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-24* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *10 July 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

Detailed Action

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:
A person shall be entitled to a patent unless –

> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

1. Claim 24 is rejected under 35 U.S.C. 102(e) as being anticipated by Persico (US 5,574,755).

Regarding **claim 24**, Persico teaches an apparatus [Fig. 4] comprising a mixer [21], including a local oscillator input [the input to mixer 21 from local oscillator LO, LON, Fig. 4]; and a limiter [limiting amplifier 53, Fig. 4] having an output coupled to said LO input of said mixer [the 53 having an output coupled to the local oscillator input of mixer 21 for sending amplified local oscillator signal to mixer 21, col. 4, lines 13-30].

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 1, 8-10, 13 are rejected under 35 U.S.C. 103(a) as being unpatentable over Nakano (US 5,960,334 in view of Jin et al. (US 6,904,266 B1).

Regarding **claim 1**, Nakano teaches a local oscillator circuit [Fig. 1] comprising a first LO source to generate a first periodic signal cycling at a first frequency [the first period signal cycling at 800 MHz of a first local oscillator source 4, Fig. 1, col. 4, lines 2-40],

a second LO source to generate a second periodic signal cycling at a second frequency different than said first frequency [the period signal cycling at 1600 MHz of a second local oscillator source 5, Fig. 1, col. 4, lines 2-40],

a limiter [the amplification circuit between switch 23 & mixer 3, Fig. 1, col. 4, lines 2-40 & col. 5, lines 20-35; for amplifying selected local oscillator frequency of 800 MHz, according to the switched capacitance associated with switch 35, to provide greater gain for 800 MHz than the gain for 1600 MHz, to isolate the leakage signal of second LO source 1600 MHz, which is equivalent to the limiter described in applicant's specification, the providing of large gain to amplify for a selected LO signal in order to isolate the unselected LO signal, applicant's specification, paragraph 0008 in page 3 & paragraph 0026 in page 6];

a first switch element [23] to selectively couple said LO source [4] to said limiter [the amplification circuit between switch 23 and mixer 3, Fig. 1];

Nakano fails to teach a second switch element to selectively coupled said second LO source to said limiter. Jin et al. (Jin) teaches these features [a transmitter 20 comprising a second switching element 74 to selectively coupled said second local oscillator LO2 to an amplifier A3 or A4, col. col. 7, lines 1-20, Fig. 7], in order to attenuate the signal leakage [col. 2, lines 34-40]. Therefore, it would have been obvious to one of ordinary skill in the art at the time of invention to modify Nakano with Jin's second switch element 74, in order to provide isolation of the signal leakage from the unselected LO signal.

Regarding **claim 8**, Nakano teaches a method [abstract, col. 2, lines 2-40] comprising

generating a first LO signal cycling at a first frequency [the first period signal cycling at 800 MHz of local oscillator 4, Fig. 1, col. 4, lines 2-40],

generating a second LO signal cycling at a second frequency different than said first frequency [the period signal cycling at 1600 MHz of local oscillator 5, Fig. 1, col. 4, lines 2-40],

activating a first switch element [23] to substantially produce said first LO signal at a node [to substantially produce first LO signal from 4 at capacitor node 21]

amplifying said first LO signal [800 MHz] and said leakage LO signal [1600 MHz] at node [capacitor node 21], wherein a gain associated with said first LO signal is greater than a gain associated with said leakage LO signal [the amplification circuit between switch 23 & mixer 3, Fig. 1, col. 4, lines 2-40 & col. 5, lines 20-35; for amplifying selected local oscillator frequency of 800 MHz, according to the switched capacitance associated with switch 35, to provide greater gain for 800 MHz than the gain for 1600 MHz];

Nakano fails to teach the de-activating a second switch element to substantially de-couple said second LO signal from said node, wherein a leakage LO signal is also produced ate said node. Jin teaches the de-activating a second switch element [74, Fig. 7] to substantially de-couple said second LO signal [LO2] from said node [input of A4], wherein a leakage LO signal is also produced ate said node [A4, col. col. 7, lines 1-20, Fig. 7], in order to attenuate the signal leakage [col. 2, lines 34-40]. Therefore, it would have been obvious to one of ordinary skill in the art at the time of invention to modify Nakano with Jin's second switch element 74, to provide isolation of the signal leakage of the unselected LO signal.

Regarding **claim 9**, Nakano teaches amplifying said first LO signal [4, 800 MHz] and said leakage LO signal [5, 1600 MHz] is performed by a limiter [amplifying circuit between 21 and 3, Fig. 1].

Regarding **claim 10**, Nakano teaches a receiver [Fig. 1, col. 3, lines 58-65] comprising

a mixer 3 to down convert a received rf signal to an IF signal [Fig. 1]; and

a local oscillator circuit [Fig. 1] coupled to said mixer 3, wherein said LO circuit comprising:

a first LO source to generate a first periodic signal cycling at a first frequency [the first period signal cycling at 800 MHz of local oscillator 4, Fig. 1, col. 4, lines 2-40],

a second LO source to generate a second periodic signal cycling at a second frequency different than said first frequency [the period signal cycling at 1600 MHz of local oscillator 5, Fig. 1, col. 4, lines 2-40],

a limiter [the amplification circuit between switch 23 & mixer 3, Fig. 1, col. 4, lines 2-40 & col. 5, lines 20-35; for amplifying selected local oscillator frequency of 800 MHz, according to the switched capacitance associated with switch 35, to provide greater gain for 800 MHz than the gain for 1600 MHz, which is equivalent to the limiter described in applicant's specification, to provide large amplification for a selected LO signal in order to isolate the unselected LO signal, applicant's specification, paragraph 0008 in page 3 & paragraph 0026 in page 6];

a first switch element [23] to selectively couple said LO source [4] to said limiter [the amplification circuit between switch 23 and mixer 3, Fig. 1];

Nakano fails to teach a second switch element to selectively coupled said second LO source to said limiter. Jin et al. (Jin) teaches these features [a transmitter 20 comprising a second switching element 74 to selectively coupled said second local oscillator LO2 to an amplifier A3 or A4, col. col. 7, lines 1-20, Fig. 7], in order to attenuate the signal leakage [col. 2, lines 34-40]. Therefore, it would have been obvious to one of ordinary skill in the art at the time of invention to modify Nakano with Jin's second switch element 74, to provide isolation of the signal leakage of the unselected LO signal.

Regarding **claim 13,** Jin teaches a low noise amplifier LNA 32 to amplify said rf signal, wherein an output of said LNA is coupled to an input of said mixer [34, Fig. 7].

3. Claims 2-3 are rejected under 35 U.S.C. 103(a) as being unpatentable over Nakano in view of Jin, as applied to claim 1 above, and further in view of Yamao et al. (US 5,231,632).

Regarding **claim 2**, Nakano& Jin fail to teach the wherein said first and/or second switching element comprising transistor. Yamao et al. (Yamao) teaches the switches SW1, Sw2 for switching local oscillators 15A, 15B, the SW1, SW2, are FET transistors, GaAsFET transistors [Fig. 6, col. 7, lines 48-63; col. 7, lines 19-47], in order to minimize switching time for handoff [col. 7, lines 55-63]. Therefore, it would have been obvious to one of ordinary skill in the art at the time of invention to modify Nakano & Jin with Yamao's GaAsFET transistor switch, in order to minimize switching time for handoff.

Regarding **claim 3**, Yamao teaches wherein said transistor comprises a field effect transistor [the utilizing GaAsFET transistor for switches, col. 7, lines 55-63].

4. Claims 4, 11, 18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Nakano in view of Jin, as applied to claims 1, 10, 17 above, and further in view of Dexter (US 6,654,595 B1).

Regarding **claims 4, 11, 18**, Nakano teaches a limiter & first switching element, Fig. 1. Jin teaches a second switching element 74. Nakano & Jin fails to teach the transformer coupled to said limiter, wherein said transformer comprises first and second differential transformer outputs.

Dexter teaches the transformer 302 receiving LO input in Fig. 3, the transformer different outputs is coupled to the limiter 130 square wave regenerator 130 [Fig. 3, col. 13, lines 13-

27], to reduce the harmonic distortion [col. 4, line 61 to col. 5, line 8]. Therefore, it would have been obvious to one of ordinary skill in the art at the time of invention to modify Nakano & Jin with Dexter's differential transformer output to limiter square wave generator to drive mixer, in order to reduce the harmonic distortion.

5. Claims 5-7, 12, 19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Nakano in view of Jin, Dexter, as applied to claims 4, 11, 18 above, and further in view Souetinov (US 6,211,718 B1).

Regarding **claims 5, 12, 19**, Nakano teaches a limiter. Dexter teaches the wherein said first control input is couple to said first differential transformer output and wherein said second control input is couple to said second differential transformer output [differential outputs to gate 310, 312, Fig. 3]. Nakano, Jin & Dexter fail to teach other features for this claim.

Souetinov teaches the 393 local oscillator drive circuit as the limiter which comprised a first differential transistor 401 having a first conduction path [collector terminal to emitter terminal of 401] and a first control input 340 to control a resistance of said first conduction path [the first control 340 controls the resistance of the conduction path from collector terminal to emitter terminal of 401];

a second differential transistor 402 having a second conduction path [collector terminal to emitter terminal of 402] and a second control input 341 to control a resistance of said second conduction path [the second control input 341 controls the resistance of the conduction path from collector terminal to emitter terminal of 402];

a first resistive element 410 coupled between said first conduction path [collector of 401] and a power supply terminal 440 [Fig. 4];

a second resistive element coupled between said second conduction path and said

power supply terminal 440; and a current source 413 between said first and second conduction paths [the first & second paths from collector to emitter of 401, 402] and a ground terminal [Fig. 4, col. 3, line 66 to col. 4, line 30], in order to provide balance local oscillator drive signals to mixer, to reduce the noise from many resistors [col. 2, lines 8-14]. Therefore, it would have been obvious to one of ordinary skill in the art at the time of invention to modify Nakano & Jin, Dexter with Souetinov's differential local oscillator drive circuit 393, in order to reduce the noise from many resistors.

Regarding **claim 6,** Souetinov teaches the wherein said first and/or second differential transistors comprises a bipolar transistor 401, 402.

Regarding **claim 7**, Souetinov teaches the wherein said first and/or second resistive elements comprises a resistor 410, 411.

6. Claims 14-16 are rejected under 35 U.S.C. 103(a) as being unpatentable over Nakano in view of Jin, as applied to claim 10 above, and further in view of Taylor et al.. (US 5,917,854).

Regarding **claim 14**, Nakano& Jin fail to teach an image reject filter to reject an image signal present in said received rf signal, wherein said image reject filter is coupled to an input of said mixer.

Taylor et al. (Taylor) teaches an image reject filter [5, Fig. 1, col. 3, lines 30-45] to reject an image signal present in said received rf signal, wherein said image reject filter is coupled to an input of said mixer [5 is coupled to the mixer 8, Fig. 1], to reject interference of the rf image signal [col. 1, lines 19-39]. Therefore, it would have been obvious to one of ordinary skill in the art at the time of invention to modify Nakano & Jin with Taylor's image reject filter, in order to reject the interference from image signal.

Regarding **claim 15,** Taylor teaches the IF filter 32 [Fig. 1] to remove undesired signals from said IF signal.

Regarding **claim 16**, Taylor teaches IF amplifier 10 to amplify said IF signal.

7. Claims 17, 20, 22-23 are rejected under 35 U.S.C. 103(a) as being unpatentable over Nakano in view of Jin et al. (US 6,904,266 B1).

Regarding **claim 17**, Nakano teaches a transmitter [the amplifying local oscillator signal of a carrier signal of a transmitter section of a portable telephone, Fig. 1, col. 1, lines 4-9],

a transmitter comprising an mixer 3 to upconvert an intermediate frequency IF signal [signal to mixer 3] to a RF signal [rf signal to antenna 1, for transmission, col. 5, lines 45-55],

a first LO source to generate a first periodic signal cycling at a first frequency [the period signal from VCO frequency 800 MHz of local oscillator 4, Fig. 1],

a second LO source to generate a second periodic signal cycling at a second frequency different than said first frequency [the period signal from VCO frequency 1600 MHz of local oscillator 5, Fig. 1, col. 4, lines 2-28],

a limiter [amplification circuit between switch 23 & mixer 3, Fig. 1, col. 4, lines 2-28; for amplifying selected local oscillator frequency of either 800 MHz or 1600 MHz, according to the position of switch 35 incorporation with position of switch 23, which is equivalent to the limiter described in applicant's specification, to provide large amplification for a selected LO signal in order to isolate the unselected LO signal, applicant's specification, paragraph 0008 in page 3 & paragraph 0026 in page 6];

a first switch element [23] to selectively couple said LO source [4] to said limiter [the amplification circuit between switch 23 and mixer 3, Fig. 1];

Nakano fails to teach a second switch element to selectively coupled said second LO source to a amplifier. Jin et al. (Jin) teaches these features [a transmitter 20 comprising a second switching element 74 to selectively coupled said second local oscillator LO2 to amplifier A3 or A4, col. col. 7, lines 1-20, Fig. 7], to attenuate the signal leakage [col. 2, lines 34-40]. Therefore, it would have been obvious to one of ordinary skill in the art at the time of invention to modify Nakano with Jin's second switch element 74, to provide isolation of the signal leakage of the unselected LO signal.

Regarding **claim 20**, Jin teaches a power amplifier [PA] to amplifier said rf signal wherein an input of said power amplifier is coupled to an output of said mixer [42, Fig. 1].

Regarding **claim 22,** Jin teaches an rf filter to remove undesired signals from rf signal [the filter after PA before B in Fig. 1].

Regarding **claim 23,** Jin teach an IF amplifier to amplify said IF signal [the IF AGC2 in Fig. 2].

8. Claim 21 is rejected under 35 U.S.C. 103(a) as being unpatentable over Nakano in view of Jin, as applied to claim 17 above, and further in view of Cheah (US 5,309,479).

Regarding **claim 21**, Nakano & Jin fail to teach an image reject filter to reject an image signal present in said IF signal, wherein said image reject filter is coupled to an input of said mixer.

Cheah teaches an image reject filter 3 to reject an image signal present in said IF signal, wherein said image reject filter is coupled to an input of said mixer [the image reject filter 3 coupled to the input of mixer 6, Fig. col. 3, lines 47-52; col. 4, lines 24-32], in order to improve spectrum purity of the transmitted signal [abstract]. Therefore, it would have been

obvious to one of ordinary skill in the art at the time of invention to modify Nakano & Jin with Cheah's IF image reject filter 3, in order to improve spectrum purity of the transmitted signal.

Conclusion

9. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Charles C. Chow whose telephone number is (571) 272-7889. The examiner can normally be reached on 8:00am-5:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Edward Urban can be reached on (571) 272-7899. The fax phone number for the organization where this application or proceeding is assigned is (571) 273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Charles Chow CC.

Decem19, 2005.